CLAIMS

What is claimed is:

1. A system comprising:

a processor; and

an integrated circuit package operatively coupled to the processor, the integrated circuit package comprising:

a substrate having a first surface and a second surface, the second surface configured to receive a plurality of solder balls thereon;

an integrated circuit die coupled to the first surface of the substrate;

a solder resist disposed on the second surface of the substrate, the solder resist having a first portion having a first surface tension and a second portion having a second surface tension, the first surface tension being higher than the second surface tension; and

a molding compound disposed on the first portion of the solder resist.

2. The system, as set forth in claim 1, wherein the substrate comprises a slot.

3. The system, as set forth in claim 2, wherein the integrated circuit die is coupled to the substrate in a board-on-chip fashion.

4. The system, as set forth in claim 1, wherein the integrated circuit die comprises one of a memory device and a microprocessor device.

5. The system, as set forth in claim 1, wherein solder balls are disposed on the second portion of the second surface.

6. The system, as set forth in claim 1, wherein the surface tension of the first portion of the solder resist is at least 31 dynes/cm.

7. The system, as set forth in claim 1, wherein the surface tension of the first portion of the solder resist is at least 54 dynes/cm.

8. An integrated circuit package comprising:

a substrate having a first surface and a second surface, the second surface configured to receive a plurality of solder balls thereon;

an integrated circuit die coupled to the first surface of the substrate;

a solder resist disposed on the second surface of the substrate, the solder resist having a first portion having a first surface tension and a second portion having a second surface tension, the first surface tension being higher than the second surface tension; and

a molding compound disposed on the first portion of the solder resist.

9. The package, as set forth in claim 8, wherein the substrate comprises a slot.

10. The package, as set forth in claim 9, wherein the integrated circuit die is coupled to the substrate in a board-on-chip fashion.

11. The package, as set forth in claim 8, wherein the integrated circuit die comprises one of a memory device and a microprocessor device.

12. The system, as set forth in claim 8, wherein solder balls are disposed on the second portion of the second surface.

13. The system, as set forth in claim 8, wherein the surface tension of the solder resist is at least 31 dynes/cm.

14. The system, as set forth in claim 8, wherein the surface tension of the solder resist is at least 54 dynes/cm.

15. A board comprising:

a substrate having a first surface and a second surface, the second surface configured to receive a plurality of solder balls thereon; and

a solder resist disposed on the second surface of the substrate, the solder resist having a first portion having a first surface tension and a second portion having a second surface tension, the first surface tension being higher than the second surface tension.

16. The board, as set forth in claim 15, wherein the substrate comprises a slot.

17. The board, as set forth in claim 16, wherein the integrated circuit die is coupled to the substrate in a board-on-chip fashion.

18. The system, as set forth in claim 15, wherein solder balls are disposed on the second portion of the second surface.

19. A method of manufacturing an integrated circuit package comprising:

(a) providing a substrate having a first surface and a second surface, the second surface configured to receive a plurality of solder balls thereon;

(b) disposing a solder resist onto the second surface of the substrate;

(c) selectively raising the surface tension of the solder resist to create a first portion of the solder resist having a first surface tension and a second portion of the solder resist having a second surface tension higher than the first surface tension;

(d) disposing a molding compound on the second portion of the solder resist; and

(e) disposing an integrated circuit die on the first surface of the substrate.

20. The method, as set forth in claim 19, wherein act (a) comprises providing a board-on-chip substrate.

21. The method, as set forth in claim 19, wherein act (c) comprises exposing the second portion of the solder resist to an activation method.

22. The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to ultraviolet energy.

23. The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to downstream plasma etching.

24. The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to reactive ion etching.

25. The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to wet chemical etching.

26. The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to radiation etching.

27. The method, as set forth in claim 19, wherein act (c) comprises exposing the second portion of the solder resist to an activation method to raise the surface tension to at least 31 dynes/cm.

28. The method, as set forth in claim 19, wherein act (c) comprises exposing the second portion of the solder resist to an activation method to raise the surface tension to at least 54 dynes/cm.

29. The method, as set forth in claim 19, wherein act (c) comprises disposing a memory device onto the first surface of the substrate.